Amendments to the Abstract:

Please replace the previous Abstract with the following Abstract:

In a matrix of non volatile memory cells integrated on a semiconductor substrate, each memory cell includes a floating gate transistor and a selection transistor formed in a first active area, while each byte includes a byte selection transistor formed in a second active area separated from the first by portions of insulating layer. A portion of a multilayer structure including a gate oxide layer, a first polysilicon layer, a dielectric layer, and a second polysilicon layer extends over the byte selection and selection transistors, forming the gate regions thereof, and further extending on a portion of insulating layer. A conductive layer is formed in an opening in the second polysilicon and dielectric layers, over the portion of insulating layer, putting the first polysilicon layer in electric contact with the second polysilicon layer. Another portion of the multiplayer structure comprises the gate region of the floating gate transistor.